Electronic Version
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Claims

[c1] 1. A method of designing an integrated circuit (IC) for signal integrity, the method comprising the steps of:

conducting a signal integrity analysis on an IC design;

identifying any field effect transistor (FET) that causes a signal integrity failure in the case that the IC design fails the signal integrity analysis; and

modifying an edge of a failing FET that is closer than a threshold distance to a well edge.

[c2] 2. The method of claim 1, further comprising the step of repeating the signal integrity analysis on the IC design to determine whether the modification corrected the signal integrity failure.

[c3] 3. The method of claim 2, further comprising the steps of:

determining whether all failing FET edges have been modified in the case that the modification does not correct the signal integrity failure; and

repeating the modifying step for another failing FET in the case that all failing FET edges have not been modified.

[c4] 4. The method of claim 3, further comprising the step of reporting that the signal integrity failure cannot be corrected by modification of an edge of any failing FET in the case that all failing FET edges have been modified.

[c5] 5. The method of claim 2, further comprising the step of reporting that the modification is required to a physical IC design in the case that the modification corrected the signal integrity failure.

[c6] 6. The method of claim 1, wherein the threshold distance indicates a distance at which the FET edge creates a well proximity effect with the well edge.

[c7] 7. The method of claim 1, wherein the modifying step includes moving the edge of a failing FET away from a respective well edge.

[c8] 8. A system for designing an integrated circuit (IC) for signal integrity, the method comprising the steps of:

means for conducting a signal integrity analysis on an IC design;

means for identifying any field effect transistor (FET) that causes a signal integrity failure in the case that the IC design fails the signal integrity analysis; and

means for modifying an edge of any failing FET that is closer than a threshold distance to a well edge.

[c9] 9. The system of claim 8, further comprising means for repeating the signal integrity analysis on the IC design to determine whether the modification corrected the signal integrity failure.

[c10] 10. The system of claim 9, further comprising:
means for determining whether all failing FET edges have been modified in the case that the modification does not correct the signal integrity failure; and
means for repeating the modifying step for another failing FET in the case that all failing FET edges have not been modified.

[c11] 11. The system of claim 10, further comprising means for reporting that the signal integrity failure cannot be corrected by modification of an edge of any failing FET in the case that all failing FET edges have been modified.

[c12] 12. The system of claim 9, further comprising means for reporting that the modification is required to a physical IC design in the case that the modification corrected the signal integrity failure.

[c13] 13. The system of claim 8, wherein the threshold distance indicates a distance at which the FET edge creates a well proximity effect with the well edge.

[c14] 14. The system of claim 8, wherein the modifying means moves the edge of any failing FET away from a respective well edge.

[c15] 15. A computer program product comprising a computer useable medium having computer readable program code embodied therein for designing an integrated circuit (IC) for signal integrity, the program product comprising:

program code configured to conduct a signal integrity analysis on an IC design;

program code configured to identify any field effect transistor (FET) that causes a signal integrity failure in the case that the IC design fails the signal integrity analysis; and

program code configured to modify an edge of any failing FET that is closer than a threshold distance to a well edge.

[c16] 16. The program product of claim 15, further comprising:

program code configured to repeat the signal integrity analysis on the IC design to determine whether the modification corrected the signal integrity failure; and

program code configured to report the modification is required to a physical IC design in the case that

the modification corrected the signal integrity failure.

[c17] 17. The program product of claim 16, further comprising:

program code configured to determine whether all failing FET edges have been modified in the case that the modification does not correct the signal integrity failure; and

program code configured to repeat the modifying step for another failing FET in the case that all failing FET edges have not been modified.

[c18] 18. The program product of claim 17, further comprising program code configured to report that the signal integrity failure cannot be corrected by modification of an edge of any failing FET in the case that all failing FET edges have been modified.

[c19] 19. The program product of claim 15, wherein the threshold distance indicates a distance at which the FET edge creates a well proximity effect with the well edge.

[c20] 20. The program product of claim 15, wherein the modifying program code moves the edge of any failing FET away from a respective well edge.